

## Architectural Techniques for Improving NAND Flash Memory Reliability

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**VENUE** CS Seminar Room, Y6405  
6th Floor, Yellow Zone  
Yeung Kin Man Academic Building  
City University of Hong Kong  
83 Tat Chee Avenue  
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### ABSTRACT

Raw bit errors are common in NAND flash memory and will increase in the future. These errors reduce flash reliability and limit the lifetime of a flash memory device. We aim to improve flash reliability with a multitude of low-cost architectural techniques. We show that NAND flash memory reliability can be improved at low cost and with low performance overhead by deploying various architectural techniques that are aware of higher-level application behavior and underlying flash device characteristics.

We analyze flash error characteristics and workload behavior through experimental characterization, and design new flash controller algorithms that use the insights gained from our analysis to improve flash reliability at a low cost. We investigate four directions through this approach. (1) We propose a new technique called WARM that improves flash reliability by 12.9 times by managing flash retention differently for write-hot data and write-cold data. (2) We propose a new framework that learns an online flash channel model for each chip and enables four new flash controller algorithms to improve flash reliability by up to 69.9%. (3) We identify three new error characteristics in 3D NAND through a comprehensive experimental characterization of real 3D NAND chips, and propose four new techniques that mitigate these new errors and improve 3D NAND reliability by up to 66.9%. (4) We propose a new technique called HeatWatch that improves 3D NAND reliability by 3.85 times by utilizing self-healing effect to mitigate retention errors in 3D NAND.

### BIOGRAPHY

Yixin Luo received the B.S.E. degree in computer engineering from the University of Michigan, Ann Arbor, MI, USA and the B.S.E. degree in electrical engineering from Shanghai Jiao Tong University, and the Ph.D. degree in computer science at Carnegie Mellon University. At Carnegie Mellon, he is involved in research on DRAM and flash reliability, and on datacenter reliability and cost optimization. Mr. Luo received the Best Paper Award and the Best Paper Runner-Up Award from the IEEE International Symposium on High-Performance Computer Architecture in 2012 and 2015, respectively, and the Best Paper Award from the DFRWS Digital Forensics Research Conference Europe in 2017. For more information about Yixin, please visit his website: <http://www.cs.cmu.edu/~yixinluo/>.

**All are welcome!**



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